

Interleaving Technique in Multiphase Buck & Boost Converter

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Abstract— Some of the recent applications in the field of the power supplies use multiphase converters to achieve fast dynamic response, smaller input/output filters or better packaging. Typically, these converters have several paralleled power stages with a current loop in each phase and a unique voltage loop. The presence of the current loops is necessary to increase dynamic response (by using Current mode control) and to avoid current unbalance among phases.

IndexTerms—Multiphase Buck, Self balance Mechanism, Zero voltage Switching.

I. INTRODUCTION

Interleaving technique was proposed long time ago [1-2]. In the last years, some applications make use of this technique to improve the performance of the dc-dc conversion. Dynamic response of VRMs is improved with it [3-4]; also, automotive 42/14V systems use it to reduce the size of input and output capacitors [5-7]; and other applications take advantage of this technique to improve a particular characteristic [8]. Most of the published papers regarding multiphase converters include a current loop in each phase to achieve two objectives: (a) Improve dynamic response: by using a current mode control, a higher bandwidth can be achieved. (b) Balance the phase currents: dc currents differences are restored by the control.

Each current loop needs several components increasing the cost of the power supply. Due to this, the number of phases is limited to 3 to 5 typically. Commercial ICs have been recently developed to offer a compact solution. Moreover, multiphase converters allow bandwidths near Mf_s (M times the switching frequency) being M the number of phases. However, there are many applications that do not require a very fast dynamic response, being possible to get rid of current loops. In CCM (Continuous Conduction Mode), the current unbalance depends mainly on duty cycle differences and parasitic resistance. Under certain limits allowing the operation of the converter without the mentioned current loops. Since the duty cycle is the main responsible of the current unbalance, it is especially the use of digital control that reduces the inequalities of the driving signals of the power MOSFETs. The use of a high number of phases

together with digital control without current loops has been used successfully in static conditions.

Section II presents the techniques of Self balancing Technique. Features and theory of a Multiphase Buck converter used in this work are discussed in Section III. Current balancing in multiphase converter is described in the next section. Section V provides the Balancing Technique adopted in this work. Simulink model for the chosen Converter is explained in Section VI along with results. Section VII concludes the paper.

II. MULTIPHASE BUCK CONVERTER

This paper proposes a design for the power stage in CCM that improves the current balance without using current loops. If this were possible, designs with a high number of phases would become a realistic option in some applications. The main advantage of this approach is that phase currents are cancelled obtaining advantage in filter reduction and dynamic response (because L can be reduced). Including a current loop is relative expensive because of the required electronic circuitry (sensor or resistor plus differential amplifier or current transformer) and a more complex control (M current loops). Therefore, the use of a high number of phases is not cost effective. The fact of having M current loops limits the existence of multiphase converters with a high number of phases. If current loops are not included, it is necessary to oversize all the phases to foresee certain current unbalance, depending on some parameters, especially parasitic resistance and duty cycle [11], in CCM (continuous conduction mode). An interesting option that helps to reduce current unbalance is to design the converters with a phase current ripple higher than twice the average current value ($k>200\%$), this option is only possible if the buck converter is synchronous. Note that although there is a higher current ripple per phase, the interleaving technique considerably reduces the current ripple at the output. Moreover, if the number of phases of a multiphase converter were high, the waveforms tend toward this particular design because the average dc current per phase is small. There are some advantages of this design: Current balance is better (it will be explained in the next section) _ There is a natural Zero Voltage Switching (ZVS) in both transitions. The proposed interleaving approach not

only results in cancellation of the current ripple generated at the output of each converter cell, but also increases its effective ripple frequency, and thus reduces by a factor of 10 the output filter capacitor requirement. The multiphase approach were demonstrated in the prototype hardware, which showed a six fold improvement in power density, a threefold reduction in profile, and a fourfold improvement in its **transient response**.

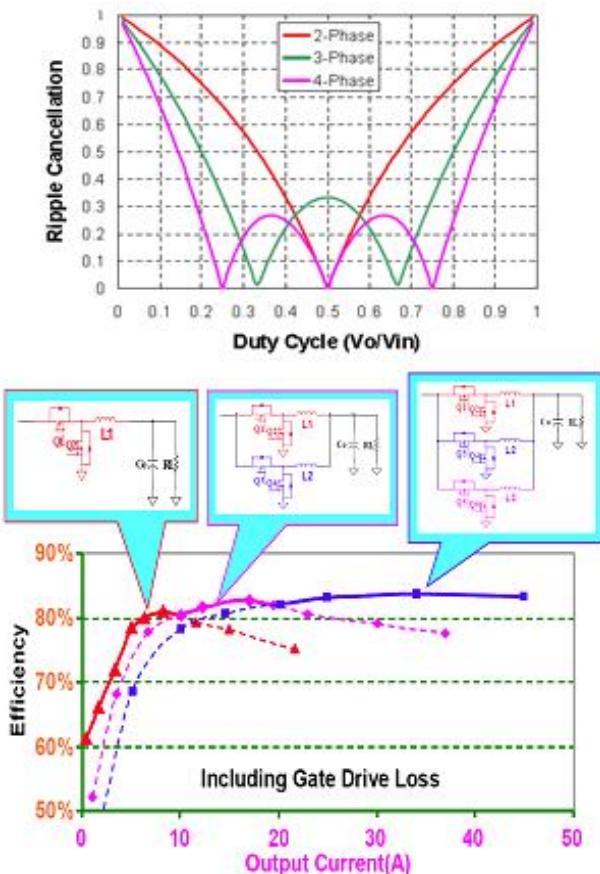


Fig.1.Efficiency improvement by applying optimal number of phases

III. SELF BALANCE OF THE PHASE CURRENT

Each buck converter has two switches the one that connects the input to the inductor (high side MOSFET or HSM) and the one that connects the inductor to ground (low side MOSFET or LSM). ZVS is achieved naturally in the turn on of LSM with a proper timing of the gate signal of these transistors. In typical designs, the turn-on of the HSM is dissipative since the inductor current is always positive and there is no way to charge/discharge the parasitic capacitances. In case of designing the converter to have negative current in that transition, ZVS is achieved, with a similar mechanism. It will be seen that this also helps to improve the current balance without current loops A, VDS, LSM and i_L are shown. When the turn-on of HSM takes place with ZVS, the speed of the charge/discharge of the parasitic capacitances is determined by the instantaneous inductor current and not by the gate-source signal of HSM. Therefore, a more (instantaneous) negative current produces a quicker

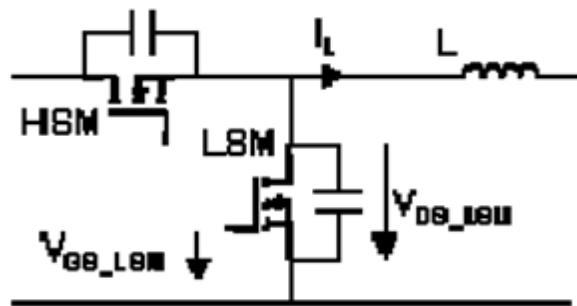


Fig 2.Power stage of Synchronous buck converter

transition increasing the voltage second balance on the inductor and then increasing the average inductor current. This mechanism tries to compensate current unbalances since the phase with the smallest dc current polarizes more its inductor and, as a consequence, the dc current is increased. On the other hand, smaller the instantaneous current, the higher the switching interval. This is a well-known issue but the important thing is that this fact helps to compensate different dc currents in a multiphase converter. Thus, the phase with the most negative current changes its inductor voltage faster and, therefore, it tries to increase its average current value. The experimental results are shown in the next section .

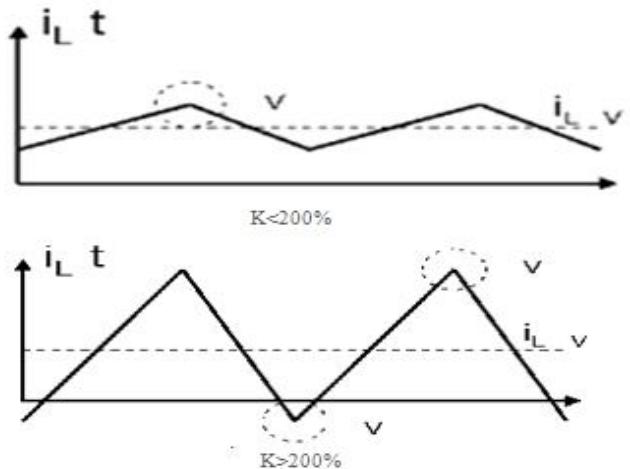


Fig 3 Current phases and parameters K for two different designs

There are some advantages of this design:

- Current balance is better
- There is natural Zero Voltage Switching (ZVS) in both transitions.

IV. EXPERIMENTAL VERIFICATION

A 4-phase synchronous buck converter without current loops has been built and tested. The main specifications are: VIN=28V; VO=12V; PO=60W; and fS=250 kHz. The inductor has been designed to obtain a current ripple higher (but close) to 200% of the average phase current (current ripple equal to 2.5A being 1.25A the average phase current). In this condition, the instantaneous phase current is negative once the LSM is opened. Figure 5 shows the phase currents for IO=5.5A ($k<200\%$) and 4.7A ($k>200\%$). In both cases, the currents are

well balanced mainly because a digital control has been used, so there is high accuracy in the timing of the driving signals. However, if the current ripple is so high that there is negative current in the turn-off of the LSM, the balance is improved. In table I we can see that, with this design, phase #1 improves from +6% over current to +3%. To test the goodness of this design, an external 0.5% extra duty cycle has been applied to phase #4 (the control is implemented in a FPGA and this can be done easily). Note that differences in the duty cycle are the main responsible for current unbalance.

If $k < 200\%$ there is an obvious current unbalance, forcing to a 67% over current in the phase this extra duty cycle (note that 0.5% duty cycle unbalance is a realistic value for many analog controllers). Of course, this result is not acceptable. However, designing with $k > 200\%$, the current unbalance is still very good even with this extra duty cycle phase #4 handles only 8% extra current, being the converter well balanced even when there is a large duty cycle unbalance. Additional experiments have been carried out introducing a much higher extra duty cycle in four phases. Waveforms with $k > 200\%$ are shown in figure 7. As it can be seen, the current balance is still very good. In worst case, with a 2% extra duty cycle, four phase carries +11% over current. From these experiments, it can be concluded that designing with $k > 200\%$ improves the current balance in multiphase converters.

VI. SIMULINK MODEL OF CHOSEN BUCK & BOOST CONVERTER

The main specifications are: $V_{IN} = 28V$; $V_o = 12V$; $P_o = 60W$; and $f_s = 250$ kHz for buck converter. For Boost converter $V_{IN} = 8V$; $V_O = 12V$; $I_L = 18A$. The inductor has been designed to obtain a current ripple higher (but close) to 200% of the average phase current (current ripple equal to 2.5A being 1.25A the average phase current). In this condition, the instantaneous phase current is negative once the LSM is opened. Figure 5 shows the phase currents for $I_o = 5.5A$ ($k < 200\%$) and $4.7A$ ($k > 200\%$). The zero voltage switching is the main factor to achieve the self balancing technique. By turning OFF the LSM, the inductor current will become negative because of designing the converters with a phase current ripple higher than twice the average current value.

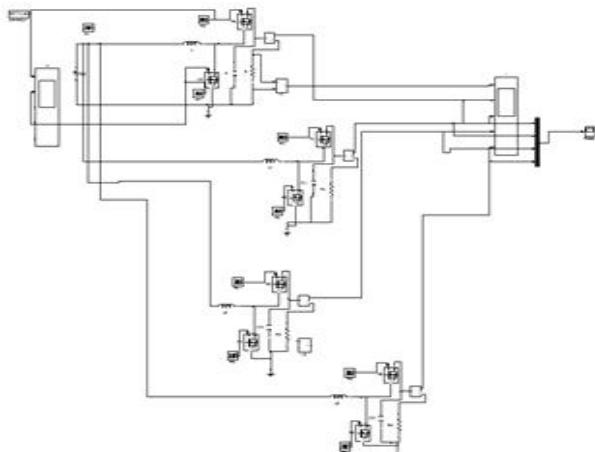


Fig. 4 Simulink model of Multi phase boost converter

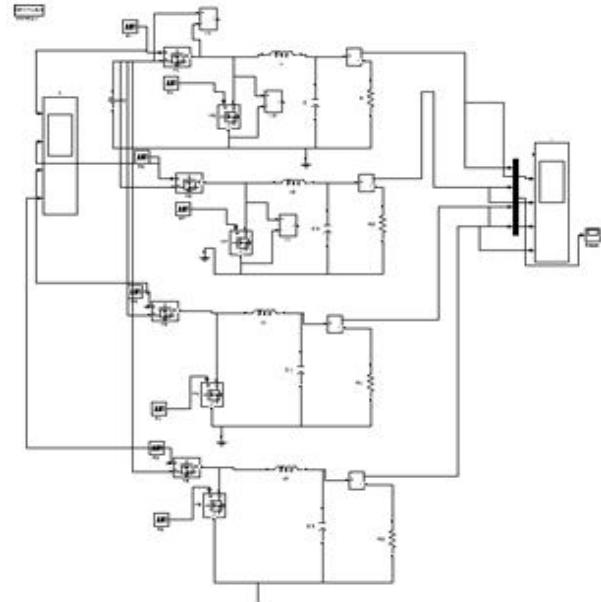


Fig 5. Simulink subsystem for Multiphase buck converter

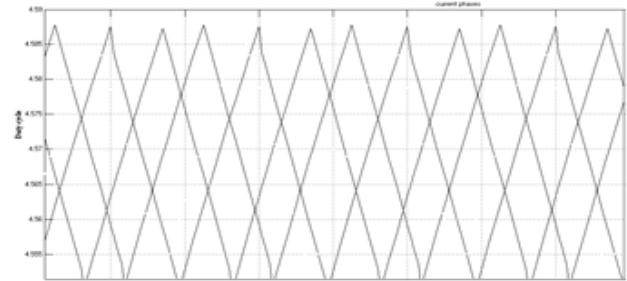


Fig 6 shows the current waveforms of 4 phase boost converter with 0.5% extra duty cycle with $K > 200\%$

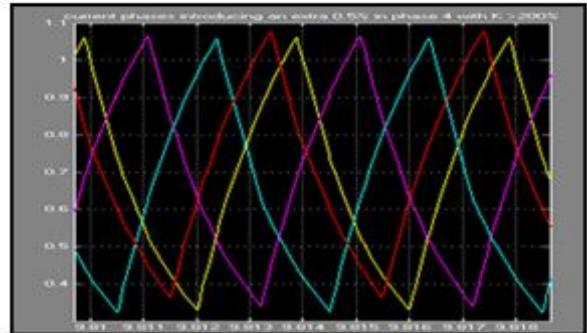


Fig 7 shows the current waveforms of 4 phase buck converter with 0.5% extra duty cycle with $K > 200\%$

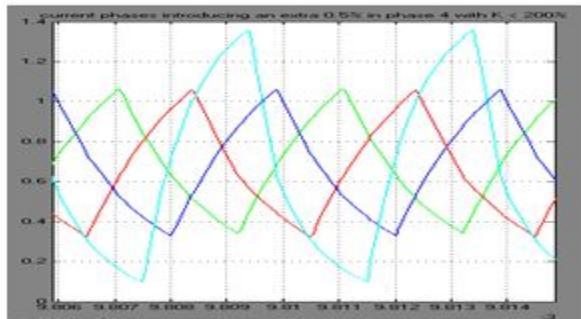


Fig 8 .The current waveforms of 4 phase buck converter with 0.5% extra duty cycle with $K < 200\%$

V. HARDWARE IMPLEMENTATION OF MULTIPHASE BUCK CONVERTR

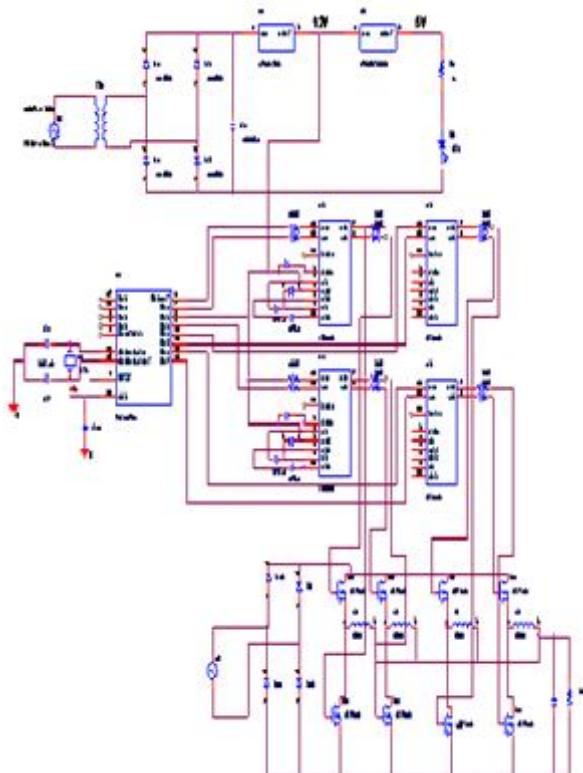


Fig.9. Simulink design for multiphase buck converter

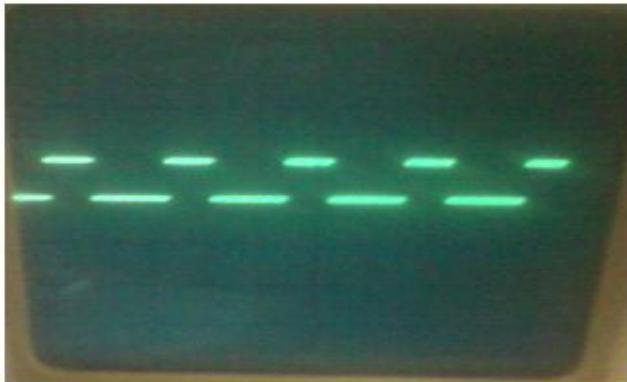


Fig.10. PWM GATE SIGNAL FOR MOSFET using CRO

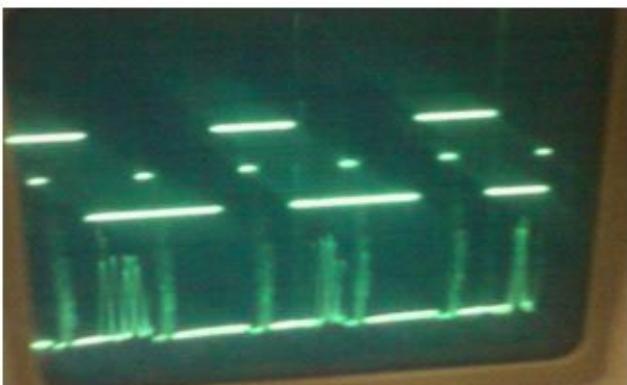


Fig.11. ZVS OF VGS & VDS OF MOSFET

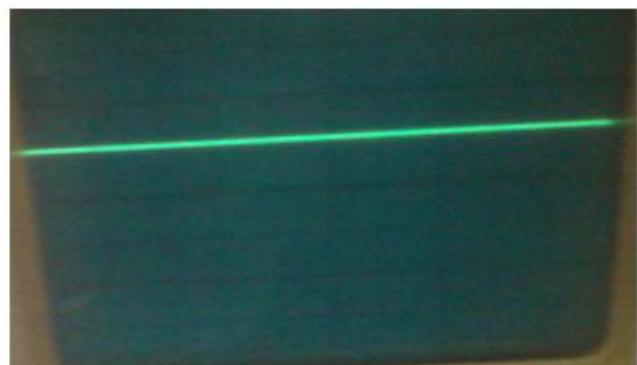


Fig.12. Output DC Voltage of Multiphase Buck Converter



Fig.13. Hardware Protocol

VI. CONCLUSION

Multiphase buck & boost converters have one current loop per phase to achieve current balance and high dynamic response. However, with a proper design, those current loops can be removed allowing cost-effective converters with a high number of phases. Designing with a current ripple higher than twice the average phase current, two important issues are achieved: better current balance and ZVS in both transitions. The instantaneous negative current during turn-off of free-wheeling MOSFET, helps to compensate differences in dc currents. On the other hand, higher conduction losses will take place and, therefore, this decision should be taken with care depending on the specifications. These results have been tested with a prototype showing very good current balance even introducing an artificial duty cycle unbalance in the control stage. Since current loops are expensive, once the current loops have been removed, it is feasible to think in multiphase converters with a high number of phases .

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